# Notice of References Cited

Application/Control No. 09/683,546	Applicant(s)/Pate Reexamination HAYES, JERRY	
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### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	А	US-6,584,606	06-2003	Chiu et al.	716/10
	В	US-			
	С	US-			
	D	US-			
	Е	US-			
	F	US-			
	G	US-			
	Н	US-			
	ı	US-			
	J	US-			
	к	US-			
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## **FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	s					
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## **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	U	P.F. Tehrani et al., Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS, Proceedings of Electronic Components and Technology Conference, pages 1009-1015, May 1996.				
	v	T. Zak et al., An Experimental Procedure to Derive Reliable IBIS Models, Proceedings of the 3 <sup>rd</sup> Electronics Packaging Technology Conference, pages 339-344, December 2000.				
	w	Y. Wang et al., The Development of Analog SPICE Behavioral Model Based on IBIs Model, Proceedings of the Ninth Great Lakes Symposium on VLSI, pages 101-104, March 1999.				
	×	J. D. Hayes et al., Behavioral Modeling for Timing, Noise, and Signal Integrity Analysis, IEEE Conference on Custom Integrate Circuits, pages 353-356, May 2001.				

A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

# Notice of References Cited Application/Control No. 09/683,546 Examiner A. M. Thompson Applicant(s)/Patent Under Reexamination HAYES, JERRY D. Art Unit Page 2 of 2

## **U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-			
	В	US-			
	С	US-			
	D	US-			
	Е	US-			
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	G	US-			
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	К	US-			
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## **FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	Р					
	ø					
	R					
	S					
	Т					

## **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	J.D. Hayes et al., Using Voltage and Temperature Adders To Account for Variations in Operating Conditions During Digital Timing Simulation, Tenth Annual IEEE International ASIC Conference and Exhibit, pages 348-351, September 1997.
	٧	B. Ackalloor et al., An Overview of Library Characterization in Secmi-Custom Design, IEEE 1998 Custom Integrated Circuits Conference, pages 305-312, May 1998.
	w	I.S. Stievano et al., Behavioral Modeling of Digital IC Input and Output Ports, Electrical Performance of Electronic Packaging, pages 331-334, October 2001.
	х	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYYY format are publication dates. Classifications may be US or foreign.